SPACE-QUALIFIED TRANSCEIVER FOR SINGLE-LINK SPACE WIRE INTERCONNECT

Session: Space Wire Components

Long Paper

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ABSTRACT

Space Wire (SW) protocol utilizes the so-called data/strobe encoding that requires two differential links per one interconnect channel. Transmission of synchronized signals through two independent physical links represents a major challenge and limits the achievable speed of the interconnect. This paper presents a new SW-compatible multi-gigabit interconnect technique that allows for both data and clock transmission through one physical link using three-level voltage pulses. Within this technique, the transmitter increases the amplitude of each odd bit of the serial data stream in either direct or inverted channel of a differential link. These overhead pulses are detected by the receiver and converted into the required divided-by-2 clock signal, while differential data bits are received in the usual way and latched in by the reconstructed clock. The proposed technique does not require changes in the SW protocol and can be implemented in any SW system. The feasibility of the proposed approach has been verified through fabrication of a transceiver test chip in a SiGe BiCMOS technology. The chip has demonstrated a reliable operation at data rates above 1*Gb/s* under normal or space-like conditions. The unused second link of a standard SW interconnect can by used as a redundant data channel. Special link integrity control algorithm and circuit have been developed to provide real-time monitoring and activation of the functional link on both transmitter and receiver sides. The complete transceiver chip has been designed in the mentioned BiCMOS technology.