GR712 – A MULTI-PROCESSOR DEVICE WITH SPACEWIRE INTERFACES

Session: SpaceWire Components

Short Paper

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ABSTRACT

The GR712 device is a first of its kind, offering the space community powerful multi-core processor capability in combination with multiple RMAP enabled SpaceWire links. The device is highly configurable and can operate in many different applications, ranging from platform control to payload processing.

The main functions of the GR712 device are:

- 2 x LEON3FT 32-bit SPARC V8 Processor with
  - IEEE-754 High-performance Floating Point Unit
  - SPARC V8 Reference Memory Management Unit
  - 4x4kByte Instruction Cache, 4x4kByte Data Cache
  - Branch prediction
- Debug Support Unit with JTAG Debug Interface
- 6 x SpaceWire links, of which two with RMAP
- 10/100 Mbit/s Ethernet MAC
- Redundant Mil-Std-1553B BC/RT/MT (A/B)
- 2 x CAN 2.0B
- I^2C and SPI interfaces
- 8 x Timers, 6 x UARTs, Interrupt Controller, General Purpose Input/Output
- CCSDS/ECSS Telemetry and Telecommand
- 192 kByte On-chip SRAM with ECC
- Memory controller for SRAM/PROM/SDRAM/IO with BCH and RS protection

The expected performance of the GR712 device at 125 MHz system clock frequency is approximately 300 Dhrystone MIPS. The expected speed of the SpaceWire links is above 250 MBPS.

The GR712 is implemented on the 180 nm Tower technology using the RadSafe™ radiation-hard-by-design library from Ramon Chip. As a preparation for this development, a first ASIC silicon prototype, the GR702, with integrated processor and SpaceWire interfaces has been successfully manufactured, validated and undergone radiation testing. The final GR712 device is expected to be latch-up free, be fully protected against single event upsets in registers and memory, and tolerate a high total ionizing dose. Prototypes are expected in 2010.

The full paper will present the GR712 device in detail; covering the SpaceWire links and how multi-processor networks can be implemented using the device.