HIGH PERFORMANCE PPC BASED DPU WITH SPACEWIRE RMAP PORT

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Short Paper

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ABSTRACT

This paper presents a high performance Data Processing Unit (DPU) with a SpaceWire RMAP Interface. Over 1000 MIPS / 800 MFLOPS performance at 800 MHz CPU clock is achieved with a high performance PowerPC CPU. The DPU has two SpaceWire links operating at up to 100 Mbits/s, one with RMAP. These are used to connect the DPU to other SpaceWire nodes. The DPU's 100 Mbits/s RMAP port can be RMAP Initiator, an RMAP Target or both. The DPU has been developed for use on the MARC demonstrator.

The SpaceWire RMAP port of the DPU is implemented by using ESA's SpaceWire RMAP IP Core. This allows that the RMAP port of the DPU supports both the Initiator RMAP Interface and Target RMAP Interface. The VHDL RMAP IP Core is integrated in the DPU system by VHDL user logic which allows CPU / user software to access all the RMAP IP functions and generates interrupts for the CPU for fluent software execution.

The RMAP IP Core along with the CPU bus interface, memory interfaces with DMA, UART and Interrupt controller are implemented in Actel Axcelerator AX2000 FPGA.