ENHANCED DYNAMIC RECONFIGURABLE PROCESSING MODULE FOR FUTURE SPACE APPLICATIONS

Session: SpaceWire missions and applications

Short Paper

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ABSTRACT

The current trend of the ever increasing detector coverage provides scientist more precise measurement results of an observed object in space. With these detectors also the data rates and amount of data to be processed by payload Data Processing Units (DPUs) increase drastically and classical ground processing steps need to be performed on-board of spacecrafts. The requirement for these advanced processing tasks by the scientist is that they have to be adapted to mission specific requirements. Today state of the art radiation tolerant SRAM-based FPGA with large gate count provide an attractive solution for in-flight and dynamic reconfigurability. With these devices an advanced system can be implemented which can even challenge future space requirements in terms of re-usability and modularity. For these enhanced systems the system reliability has to be carefully considered. With glitch effects and SEU induced errors the system can become non-deterministic and requires advanced mitigation techniques and fault tolerant communication architectures.

In this paper we will present an advanced payload architecture which provides in-flight and dynamic reconfigurability. The architecture is module based and inter connected by a SpaceWire routing network. The modules are subdivided into flexible System-on-Chip approaches with heritage from DPUs from Venus Express VMC and DAWN framing camera. On-chip communication is provided with a SpaceWire standard based high speed glitch-free communication architecture System-on-Chip Wire (SoCWire). This SoCWire interface provides also a flexible and high-speed inter-device communication. This advanced reconfigurable system is currently developed at IDA in the frame of the ESA Dynamically Reconfigurable Processing Core (DPRM) study.