FORMAL VERIFICATION FOR SPACEWIRE LINK INTERFACE USING MODEL CHECKING

Session: SpaceWire test and verification

Short Paper

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ABSTRACT

The design of the SpaceWire based satellite onboard system circuits was a part of the job in the development of Space Solar Telescope (SST) project, which has been completed by National Astronomical Observatories, Chinese Academic of Sciences. In order to prove the circuit designed for the highly reliable communication based on SpaceWire protocol was faithfully implements the SpaceWire protocol's specification, this study aimed to verify the SpaceWire link interface, which was one of the important elements of the SpaceWire. Formal verification techniques were applied during the process of development of the circuits and automated model checking approach was employed. The implementation designed as VHDL models on the FPGA for SpaceWire link interface circuit under investigation has an extension state (Error Analysis) in the state diagram providing link initialization, normal operation and error recovery services between transmitter and receiver on exchange level. All properties were checked successfully on the original model by using Formalcheck tool. The results of the verification showed that the implementation of SpaceWire link interface circuit was proved to be equivalent to the specification according to SpaceWire protocol. All these properties were also checked in SMV tool. And the differences of the performance of using these two tools were summarised. The results suggested that the SpaceWire link interface circuit implemented on FPGA is reliable and can be integrated in the SST project.