THEORY OF OPERATION AND V_{DD} FAULT SCENARIO FOR LVDS PHYSICAL LAYER OF SPACEWIRE

Session: SpaceWire Components

Long Paper

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ABSTRACT

The SpaceWire Standard ECSS-E-ST-50-12C [3] calls for a Low Voltage Differential Signaling (LVDS) physical layer as defined in ANSI/TIA/EIA-644 [1], Electrical Characteristics of Low Voltage Differential Signaling Interface Circuits. This paper will discuss that Aeroflex Colorado Springs LVDS drivers are compatible with the ANSI/TIA/EIA-644 standard and contain a current source which generates the required voltage across a 100Ω, parallel, resistor. Laboratory results will be reported which examine a hypothetical failure mode where the supply voltage, V_{DD}, exceeds the ABSOLUTE MAXIMUM RATINGS defined in the Aeroflex Datasheet [4][5][6][9].

1 BACKGROUND

Low Voltage Differential Signaling, LVDS, is useful in applications that require low power, low noise, and high-speed point-to-point communications. The SpaceWire physical layer uses Data-Strobe (DS) Encoded LVDS to communicate serial, full-duplex, bidirectional data. Figure 1 shows a notional SpaceWire Link using the LVDS physical layer, the operation of LVDS will be explained later in this paper.

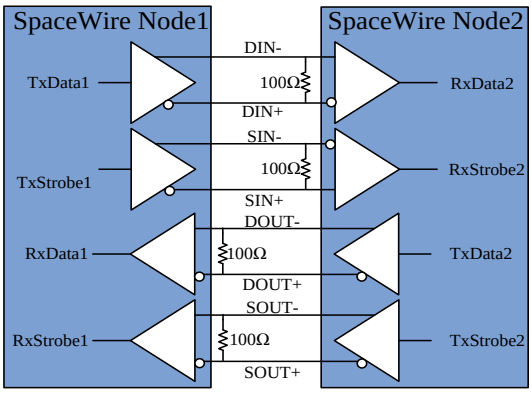

Figure 1. Single point to Point SpaceWire Link

The Input/Output signal levels are defined by ANSI/TIA/EIA-644, which is an electrical signaling standard only; it does not define a protocol. Instead, the protocol is defined in the SpaceWire Standard specification ECSS-S-ST-50-12C, which is derived from IEEE 1355-1995.

2 LVDS FUNCTIONALITY

LVDS is a method used to transmit and receive hundreds of megabits per second over differential media using a low voltage signal swing (~350mV). LVDS communications are preformed by a driver and a receiver. The driver accepts a standard Complementary Metal Oxide Semiconductor (CMOS) signal and outputs a constant current, differential, signal. The LVDS receiver senses the differential voltage across a 100Ω termination resistor and outputs a standard CMOS signal equivalent to the supply voltage. The differential aspect of LVDS allows systems to run at high data rates, with low switching power, high noise immunity, and common mode range.

The LVDS driver works by using NMOS Field Effect Transistors (FETs) to control the direction of the constant 3.5mA current source through the termination resistor. The driver current, flowing through the 100Ω termination resistor placed across the differential inputs of the receiver, generates a +/-350mV I-R drop which is sensed as a logic high/low by the receiver. The LVDS receiver has very high DC input impedance, so the majority of the driver's current flows, in a loop, from the source terminal through the 100Ω termination resistor and back into the sinking terminal.

When the driver output current direction changes, the direction of current flow across the termination resistor changes accordingly, creating the logic 1 or 0 state at the receiver output. Figure 3 shows current flow through the driver/receiver system resulting in a logic low at the receiver output. The constant current source drives +3.5mA through Q2 and into the negative half of the LVDS bus. The current reaches the termination resistor located at the receiver, flows back through the positive half of the bus, returns to the terminal drain of Q3 in the driver, and then passes into the driver VSS plane. The direction of the current flow through the termination resistor (negative to the positive), a forward voltage drop occurs and a logical low appears at the output (ROUT) of the receiver. The opposite is true for a logic high on the receiver output as shown in figure 4.

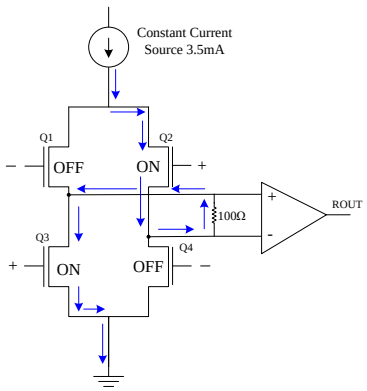

Figure 3. Logic Low (zero, 0) State

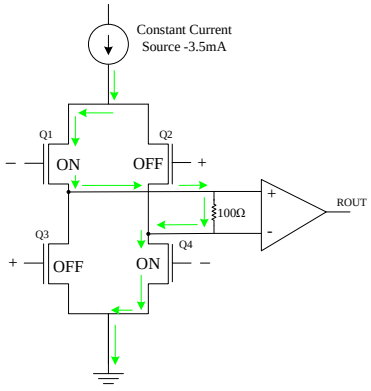

Figure 4. Logic High (one, 1) State

3 LABORATORY EXPERIMENTS OF POWER SUPPLY FAULTS [7]

UT54LVDS031LV and UT54LVDS032LV devices were used for all laboratory experiments. To demonstrate the devices response to an over voltage failure mode, experiments were performed with an 8.0V ramp on supplies and I/Os while monitoring the driver inputs (DIN), driver outputs (DOUT+/-), receiver inputs (RIN+/- across 100Ω), and receiver outputs (ROUT). All data was taken at 25°C (ambient) with either a 1 minute or 15 second dwell time at each voltage providing more than enough time for any overheating damage to present [7].

One of the experiments conducted in the lab at ambient conditions used the following test setup.

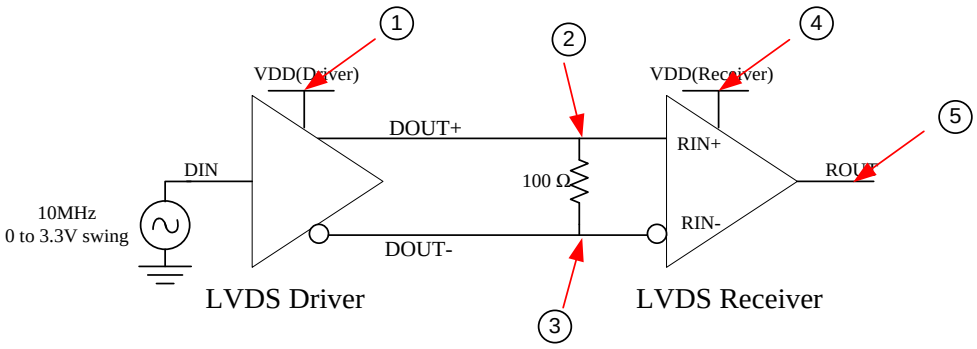

Figure 5. Example 1 Test Configuration
DIN = 10MHz with a 0 to 3.3V swing, EN = 3.3V, /EN = 0V

This test evaluated how a standard LVDS driver/receiver configuration responds to a driver power supply over voltage fault. The voltage and current of the driver and receiver power supplies was monitored. The differential output voltages on the DOUT+/RIN+ and DOUT-/RIN- signals across the 100Ω termination resistor and the output of the receiver (ROUT). VDD(Driver) was ramped from a nominal 3.3V to 8.0V. A standard lab power supply with 2.5A current limit was used for this experiment. The power supply current limiting capabilities prevented VDD on the UT54LVDS031LV driver from ramping past 8.0V.

Table 1. Example 1 Test Results

VDD(Driver)	**I VDD(Driver)**	**DOUT+**	**DOUT-**	**VDD(Receiver)**	**I VDD(Receiver)**	**ROUT**
(V) Point 1	(mA) Point 1	(V_{AVG}) Point 2	(V_{AVG}) Point 3	(V) Point 4	(mA) Point 4	(V_{AMP}) Point 5
3.3	12.49	1.30	1.41	3.3	6.66	3.12
3.6	13.17	1.33	1.44	3.3	6.63	3.04
4.0	13.73	1.35	1.46	3.3	6.62	3.20
5.0	15.95	1.47	1.56	3.3	6.56	3.02
6.0	23.31	1.83	1.92	3.3	6.54	3.20
7.0	261.0	2.51	2.61	3.3	6.07	3.12
8.0	500.0	2.38	3.20	3.3	10.50	3.42

Table 1 indicates that the standard LVDS driver/receiver configuration did not propagate a high voltage fault when VDD on the driver is ramped to 8.0V. The maximum voltage seen on the DOUT+/RIN+ and DOUT-/RIN- signals are within the absolute maximum ratings for both devices. The high voltage stress on the driver

VDD permanently damaged the driver device without propagating the fault to the receiver. The UT54LVDS032LV receiver continued to function after the fault condition.

The next experiment conducted in the lab at ambient conditions used the following test setup.

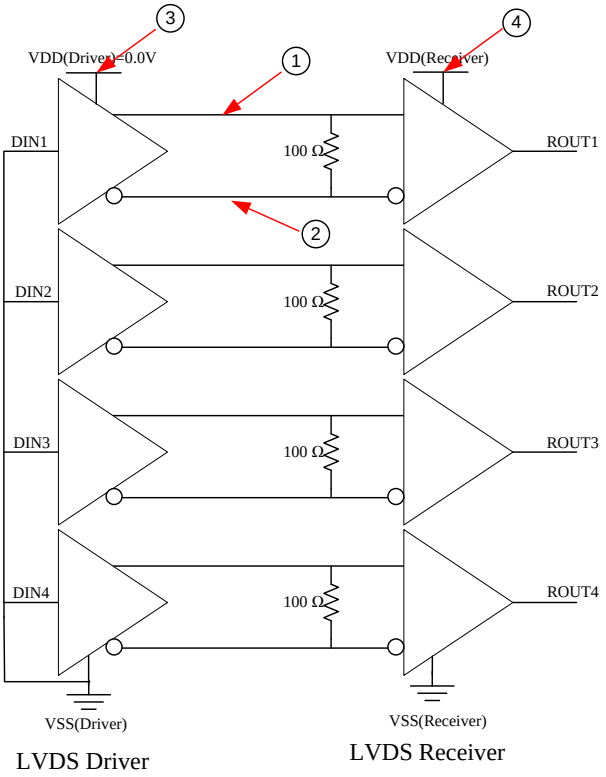

Figure 6. Example 2 Test Configuration
EN = /EN = 0.0V

This test evaluated the differential lines (DOUT+/RIN+ and DOUT-/RIN-) with the receiver powered and the driver unpowered (cold spare mode). The inputs of the driver (DIN) were set to 0.0V and the supply voltage of the receiver, VDD(Receiver), was ramped to 8.0V. The voltage and current of the receiver and driver power supplies and the +/- differential signals were monitored.

Table 2. Example 2 Test Results

VDD(Receiver)	**I VDD(Receiver)**	**VDD (Driver)**	**I VDD(Driver)**	**DOUT1+**	**DOUT1-**
(V) Point 4	(mA) Point 4	(V) Point 3	(mA) Point 3	(V_{AVG}) Point 1	(V_{AVG}) Point 2
3.3	9.54	0.0	0.07	1.23	1.45
3.6	10.11	0.0	0.11	1.93	1.93
4.0	10.87	0.0	.10	2.72	2.73
5.0	15.71	0.0	0.08	4.83	4.81
6.0	15.71	0.0	0.08	5.83	5.82
7.0	17.86	0.0	0.11	6.80	6.77
8.0	19.70	0.0	0.11	0.20	0.24

Table 2 indicates this standard LVDS driver/receiver configuration does propagate receiver supply over voltages. Although over voltages can propagate, faults are not propagated based on further analysis. Additionally, at 8V the voltage on the LVDS inputs drops significantly indicating the receivers experience catastrophic failure but the voltage out of the LVDS inputs remains within the recommended operating range when VDD exceeds approximately 8V.

Another example experiment conducted in the lab at ambient conditions used the following test setup.

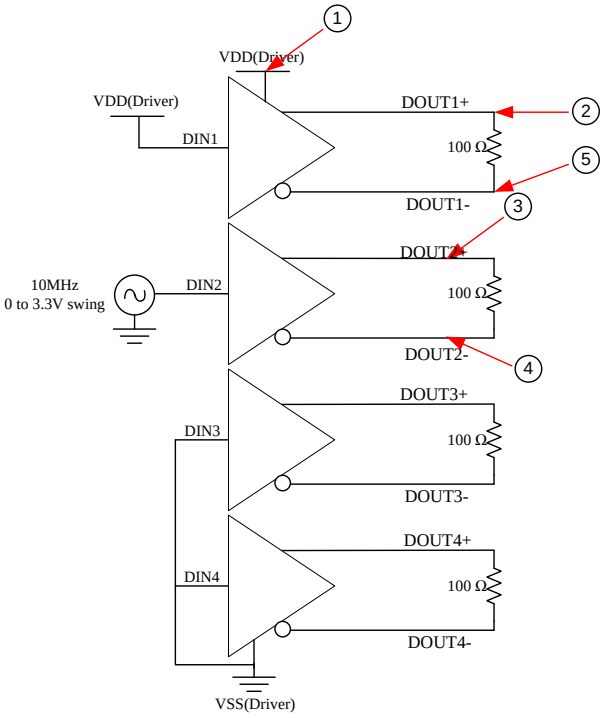

Figure 7. Example 3 Test Configuration
EN = 3.3V, /EN = 0V
DIN1 = VDD(Driver) DIN2 = 10MHz with a 0 to 3.3V swing DIN3 = DIN4 = VSS = 0.0V

This test evaluated the differential line (DOUT+ and DOUT-) performance when VDD of the driver was ramped from 0.0V to 8.0V. This was accomplished by setting the enable signals on the UT54LVDS031LV to EN=3.3V and /EN=0.0V. Input #1 (DIN1) was set to VDD(Driver), input #2 (DIN2) was stimulated with a 10MHz square wave with 0.0 to 3.3V peak-to-peak, and inputs #3 and #4 were set to 0.0V. The voltage and current of the driver power supply, voltage across the termination resistor across DOUT1, voltage at DOUT1+, voltage at DOUT2+, and voltage at DOUT2- were monitored.

Table 3. Example 3 Test Results

VDD(Driver)	I VDD(Driver)	DOUT1+	DOUT2-	DOUT2+	DOUT1+/-
(V) Point 1	(mA) Point 1	(V_{AVG}) Point 2	(V_{AVG}) Point 3	(V_{AVG}) Point 2	(V_{AVG}) Point 2
3.3	16.48	1.36	1.10	1.40	0.34
3.6	17.07	1.42	1.10	1.36	0.35
4.0	17.91	1.45	1.41	1.07	0.37
5.0	24.61	1.61	1.29	1.53	0.42
6.0	86.08	2.12	1.82	1.82	0.62
7.0	169.31	3.64	3.18	2.16	1.16
8.0	758.81	0.54	0.58	0.60	0.00

Table 2 indicates the UT54LVDS031LV does not propagate supply over voltages when the voltage on the LVDS input pin is within the recommended range (DOUT2) but does propagate over voltages when the LVDS input pin follows the supply overvoltage (DOUT1). The voltage across DOUT1's resistor scales proportionally with the overvoltage, showing increasing current due to increasing voltage.

Although over voltages can propagate, faults are not propagated as the current sourced by DOUT1+ is returned through DOUT1-. Insufficient current would flow into a receiver to cause damage or degradation per section 4.0. Additionally, at 8V the voltage on the LVDS lines drops significantly indicating the drivers experience catastrophic failure but the outputs fail to a voltage within the recommended operating range for VDD ≥ 8V.

The last example provided for this paper was conducted in the lab at ambient conditions used the test setup shown in figure 8.

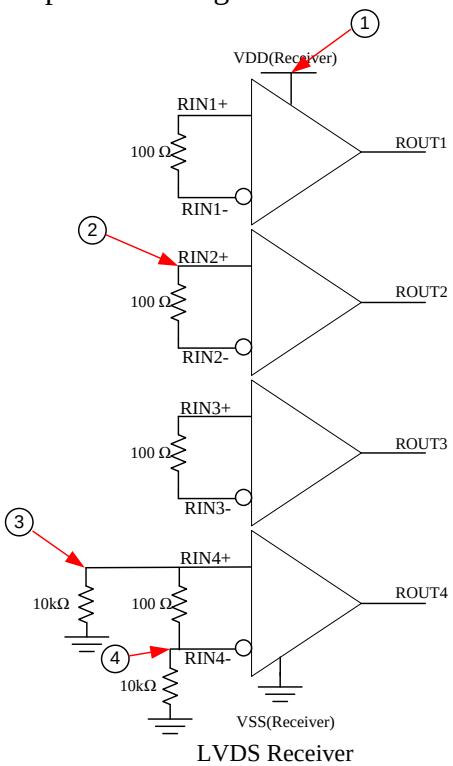

Figure 8. Example 4 Test Configuration
EN = /EN = 0V

This test evaluated the receiver differential inputs (RIN+/RIN-) performance with some inputs terminated with 100Ω resistors and one pair of inputs pulled to 0.0V (VSS(Receiver)) using 10kΩ resistors, and VDD(Receiver) was ramped from 0.0V to 8.0V. The voltage and current of the receiver power supply, and selected RIN+/RIN- inputs monitored. A standard lab power supply with 2.5A current limit was used for this experiment. Table 4 indicates the UT54LVDS032LV does propagate receiver supply over voltages out of its RIN inputs.

Table 4. Example 4 Test Results

VDD(Receiver)	**I VDD(Receiver)**	**RIN2+**	**RIN3+**	**RIN3-**
(V) Point 1	(mA) Point 1	(V_{AVG}) Point 2	(V_{AVG}) Point 3	(V_{AVG}) Point 4
3.3	7.93	2.36	0.01	0.01
3.6	7.98	3.33	0.00	0.00
4.0	8.68	3.87	0.03	0.03
5.0	13.61	4.90	0.13	0.11
6.0	33.43	5.87	0.25	0.25
7.0	84.81	6.85	0.48	0.47
8.0	1188.28	0.25	0.27	0.21

Although over voltages can propagate, faults are not propagated as there is insufficient current sourced out of the RIN pins, calculated from the voltage drop across the 10 kΩ pull-down resistors, to damage or degrade the LVDS outputs per section 4.0. Additionally, at 8V the voltage on the LVDS inputs drops significantly indicating the receivers experience catastrophic failure but the voltage out of the LVDS inputs remains within the recommended operating range when VDD exceeds approximately 8V.

This experiment shows that pull-down resistors could be used to preclude receiver supply over voltages from propagating to a driver. However, these are not necessary as there is insufficient current to propagate a fault. Also, the LVDS lines would only show the receiver supply overvoltage if the driver was tristated or powered-off, as an active driver would overpower the receiver supply over voltages and hold the LVDS lines at operating levels.

4 LVDS I/O Current Reliability Analysis

The metal current density design rules for the 0.25µm LVDS technology allow a DC current of 5.98mA on the LVDS I/O while remaining within allowed specifications**.** After reviewing the reliability assessment the UT54LVDS031LV, UT54LVDS032LV, UT200SpWPHY01, and the UT200SpW4RTR these devices can tolerate 100µA of current per pin indefinitely without damage or degradation for a 15 year mission.

Additionally, from Table 4, an LVDS receiver experiencing overvoltage could back-drive up to 57µA per LVDS line to an LVDS driver. If all four pairs of LVDS lines were connected, a total of approximately 460µA could be back-driven. 460µA is more than an order of magnitude below the 5.98mA calculated threshold. Therefore,

no faults would be propagated from an LVDS receiver experiencing over voltages to an LVDS driver.

5 FAULT CONDITIONS AND RESULTS

The fault conditions examined focus on demonstrating the response of Aeroflex LVDS drivers and receivers to voltage stress above the ABSOLUTE MAXIMUM RATING for VDD and the I/O. The tests were preformed with the UT54LVDS031LV and UT54LVDS032LV devices at room temperature (25°C).

The tests described above show that over voltages can be seen on the LVDS I/O, but that faults are not propagated because the current sourced over the LVDS lines by the part experiencing the overvoltage is not sufficient to cause damage or degradation to the other LVDS part. The experiments also show that sufficiently high voltage applied to the device resulted in transistor break down causing permanent damage with no overvoltage propagation.

The Aeroflex LVDS drivers are current mode outputs with a constant current source capable of driving a 3.5mA nominal current. The results discussed are not guaranteed by Aeroflex. Any operation outside of the ABSOLUTE MAXIMUM RATINGS, as stated in the datasheet and/or SMD may affect device reliability and performance.

6 REFERENCES

[1] Telecommunications industry Association, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits ANSI/TIA/EIA-644”, January 30, 2001.

[2] IEEE P1355, “Standard for Heterogeneous InterConnect (HIC) IEEE 1355-1995”, Conference Title, Location, June 12, 1996.

[3] ESA Publications Division, “SpaceWire Standard Document ECSS-E-ST-50-12C”, The Netherlands, July 31, 2008.

[4] Aeroflex, “UT54LVDS031LV 3.3-VOLT QUAD DRIVER Datasheet”, Colorado Springs, Colorado, February 2006.

[5] Aeroflex Colorado Springs, “UT54LVDS032LV 3.3-VOLT QUAD RECEIVER Datasheet”, Colorado Springs, Colorado, March 2006.

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[7] Barry Cook, “SPACEWIRE PHYSICAL LAYER FAULT ISOLATION” Session: Test, SpaceWire Components Short Paper, 4Links Limited, Bletchley Park, MK3 6EB, England

[8] Aeroflex Colorado Springs, "Theory of Operation and VDD Fault Scenario Application Note", Colorado Springs, Colorado, March 2010

[9] Aeroflex Colorado Springs, "UT200SpW4RTR 4-Port SpaceWire Router Datasheet", Colorado Springs, Colorado, February 2010.